IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A cross-talk cancellation method using a main signal ~~(62)~~ associated with a target track ~~(32)~~ and satellite signals ~~(61, 63)~~ associated with side tracks ~~(31, 33)~~, said main signal showing transitions ~~(X_m)~~ and runs of various lengths ~~($d_{m+1,m}$)~~ between two transitions ~~(X_m, X_{m+1})~~, said cancellation method comprising the ~~steps~~ acts of:

sampling said satellite signals to form sampled satellite signals with converters that receive a fixed clock;

[[-]] filtering said satellite signals with adaptive filters ~~(71, 73)~~ that run on a fixed clock, thereby generating filtered versions ~~(81, 83)~~ of said satellite signals,

[[-]] updating ~~the~~ coefficients of said adaptive filters by minimizing ~~the~~ a mismatch between ~~the~~ an actual run length and ~~the~~

an expected run length between the two transitions of the main signal, ~~and~~

[[-]] processing said main signal, thereby generating an improved main signal ~~(102)~~, said processing including a subtraction of said filtered versions of said satellite signals from the main signal,

providing the improved main signal to a sample rate converter driven by a bit clock,

estimating a ratio between the bit clock and the fixed clock, and

taking said ratio into account during the updating act.

2. (Original) A program comprising instructions for implementing a cross-talk cancellation method as claimed in claim 1 when said program is executed by a processor.

3. (Currently Amended) A signal processor ~~(40)~~ comprising cross-talk cancellation means ~~(42)~~ for receiving a main signal ~~(62)~~ associated with a target track ~~(32)~~ and satellite signals ~~(61, 63)~~ associated with side tracks ~~(31, 33)~~, said main signal showing

transitions ~~(X_m)~~ and runs of various lengths ~~($d_{m+1,m}$)~~ between two transitions ~~(X_m, X_{m+1})~~, said cross-talk cancellation means comprising:

[[-]] filtering means ~~(71, 73)~~ for filtering said satellite signals with adaptive filters, thereby generating filtered versions ~~(81, 83)~~ of said satellite signals,

[[-]] updating means ~~(111, 113)~~ for updating ~~the~~ coefficients of said adaptive filters by minimizing ~~the~~ a mismatch between ~~the~~ an actual ~~($d_{m+1,m}$)~~ run length and ~~the~~ an expected ~~($d^{(exp)}_{m+1,m}$)~~ run length between the two transitions of the main signal, ~~and~~

[[-]] processing means ~~(93)~~ for generating an improved main signal ~~(102)~~ from said main signal by subtraction of said filtered versions of the satellite signals from the main signal,

time recovery means for estimating a ratio between a bit clock that drives the time recovery means and a fixed clock that drives the filtering means, and for providing said ratio to said updating means, said updating means being designed to take said ratio into account for updating said coefficients.

4. (Currently Amended) ~~A~~ The signal processor as claimed in

claim 3, ~~comprising a fixed clock (55), time recovery means (130), and a bit clock (120) driven by said time recovery means,~~ wherein said fixed clock ~~being~~ is asynchronous with respect to said bit clock, and wherein said cross-talk cancellation means are operated at said fixed clock.

5. (Currently Amended) ~~A~~ The signal processor as claimed in claim 4, wherein said bit clock has a bit clock frequency and said fixed clock has a fixed clock frequency that is substantially different from said bit clock frequency such that the ratio between said bit clock frequency and said fixed clock frequency is substantially different from ~~1, said signal processor further comprising time recovery means (50-1, 50-2) for estimating said ratio and providing said ratio to said updating means, said updating means being designed to take said ratio into account for updating said coefficients~~ one.

6. (Currently Amended) An apparatus ~~(6-1, 6-2)~~ for reading a signal stored along a track on a storage medium ~~(1)~~ comprising a signal processor as claimed in claim 3.

7.(Original) An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 4.

8.(Original) An apparatus for reading a signal stored along a track on a storage medium comprising a signal processor as claimed in claim 5.